CLAIMS

1. (Original) An asynchronous wrapper comprising

- at least one input unit which is adapted to receive a request signal from outside and to indicate to the outside the reception of the request signal by the delivery of an associated acknowledgement signal, and

- a pausable clock unit which is adapted to repeatedly produce a first clock signal and deliver it to an internally synchronous circuit block associated with the asynchronous wrapper,

characterised in that

- the input unit is adapted to produce, if a request signal is applied, a second clock signal which is in a defined time relationship with the request signal and to deliver it to the internally synchronous circuit block, and

- there is provided a time-out unit which is connected to the input unit and which is adapted to suppress delivery of the first clock signal to the favour of the delivery of the second clock signal.

2. (Original) An asynchronous wrapper as set forth in claim 1 wherein the time-out unit is adapted to suppress the delivery of the first clock signal to the favor of the delivery of the second clock signal.

3. (Original) An asynchronous wrapper as set forth in claim 1 wherein the time-out unit is adapted with the expiry of a predetermined period of time after delivery of the last second clock signal to deliver a control signal for enabling the delivery of the first clock signal.

4. (Original) An asynchronous wrapper as set forth in claim 1 having a clock control unit which is connected to the clock unit and to the input unit and which is adapted to drive the clock unit for the delivery of a number of clock pulses, wherein the number of clock pulses is less than or equal to the depth of a pipeline of the associated, internally synchronous circuit block.

5. (Original) An asynchronous wrapper as set forth in claim 4 wherein the clock control unit is adapted to send a control signal for stopping to the clock unit after delivery of the necessary number of clock pulses.

6. (Original) An asynchronous wrapper as set forth in claim 1 wherein the input unit is adapted, when a request signal is applied, to deliver a control signal to the internally synchronous circuit block for enabling a data input.

7. (Original) An asynchronous wrapper as set forth in claim 1 comprising at least one output unit which is adapted to send a request signal to the outside and upon the reception of an acknowledgement signal from the outside to deliver a control signal to the internally synchronous circuit block for enabling a data output.

8. (Original) An asynchronous wrapper as set forth in claim 7 wherein the input unit and the output unit are adapted to communicate with the outside by way of a four-phase handshake protocol.

9. (Original) A globally asynchronous locally synchronous (GALS) circuit including at least one internally synchronous circuit block and a respectively associated asynchronous wrapper as set forth in claim 1.

10. (Original) A GALS circuit as set forth in claim 9 wherein connected upstream of a data input of the internally synchronous circuit block is a data latch whose operation is controlled by the input unit.

11. (Original) A method of clock control of an internally synchronous circuit block of an integrated circuit by means of an asynchronous wrapper, wherein the internally synchronous circuit block can be clock controlled by means of a first clock signal which a local clock signal generator can produce, comprising the steps:

a) pausing the delivery of the first clock signal or switching off the local generator,

b) waiting for the reception of a request signal from the outside at the input of the asynchronous wrapper,

c) delivering a second clock signal from the asynchronous wrapper to the internally synchronous circuit block in a defined time relationship with the reception of the request signal and without the aid of the local clock signal generator, and

d) waiting for the reception of a next request signal from the outside and possibly repeating the preceding step.

12. (Original) A method as set forth in claim 11 wherein, in the absence of a request signal over a predeterminable period of time (time-out), switching over is effected to the delivery of the first clock signal which is produced by means of the local clock signal generator.

13. (Original) A method as set forth in claim 12 wherein the local clock signal generator is switched off after emptying of a pipeline of the internally synchronous circuit block or after the arrival of a new request signal.

14. (New) An asynchronous wrapper as set forth in claim 6 wherein the input unit and the output unit are adapted to communicate with the outside by way of a four-phase handshake protocol.

15. (New) An asynchronous wrapper as set forth in claim 14 comprising at least one output unit which is adapted to send a request signal to the outside and upon the reception of an acknowledgement signal from the outside to deliver a control signal to the internally synchronous circuit block for enabling a data output.